IEEE 2015 VLSI TITLES

S.NO	TITLES	YEAR
1.	Aging-Aware Reliable Multiplier Design With Adaptive Hold Logic	2015
2.	Fault Tolerant Parallel Filters Based on Error Correction Codes	2015
3.	Design and Analysis of Approximate Compressors for Multiplication	2015
4.	Novel Design Algorithm for Low Complexity Programmable FIR Filters Based on Extended Double Base Number System	2015
5.	Floating-Point Butterfly Architecture Based on Binary Signed-Digit Representation	2015
6.	Implementation of Subthreshold Adiabatic Logic for Ultralow-Power Application	2015
7.	Novel Block-Formulation and Area-Delay-Efficient Reconfigurable Interpolation Filter Architecture for Multi-Standard SDR Application	2015
8.	A High-Performance FIR Filter Architecture for Fixed and Reconfigurable Applications	2015
9.	High-Speed and Energy-Efficient Carry Skip Adder Operating Under a Wide Range of Supply Voltage Levels	2015
10.	Low-Power and Area-Efficient Shift Register Using Pulsed Latches	2015

11.	Array-Based Approximate Arithmetic Computing: A General Model and Applications to Multiplier and Squarer Design	2015
12.	Recursive Approach to the Design of a Parallel Self-Timed Adder	2015
13.	Further Desensitized FIR Half band Filters	2015
14.	Design and Analysis of Inexact Floating-Point Adder	2015
15.	Scalable Verification of a Generic End-Around-Carry Adder for Floating-Point Units by Coq	2015
16.	An Efficient Constant Multiplier Architecture Based on Vertical-Horizontal Binary Common Sub-expression Elimination Algorithm for Reconfigurable FIR Filter Synthesis	2015
17.	A Generalized Algorithm and Reconfigurable Architecture for Efficient and Scalable Orthogonal Approximation of DCT	2015